

TMC2243

CMOS FIR Filter

10 x 10 Bit, 20 MHz

Features

- 20 MHz data input and computation rate
- 10 x 10 bit multiplication with 23-bit extended precision sum of products (overflow, plus 16 output and 6 guard bits)
- Up to 3 zero and 3 non-zero stages per device
- Two's complement arithmetic
- 16-bit Sum-In and Sum-Out ports for cascading
- Internal 1/2 LSB rounding
- All inputs and outputs are registered
- One coefficient update per clock cycle
- Low power consumption CMOS process
- Single +5V supply

- Available in 68-pin ceramic pin grid array and 69-pin plastic PGA packages

Applications

- FIR filters
- Adaptive filters
- Multi-bit correlation
- One and two dimension video filtering
- Radar signal processors
- One and two dimension convolution
- Arithmetic element for systolic array processors

Description

The TMC2243 is a video speed three stage 10 x 10 bit FIR (Finite Impulse Response) filter integrated circuit composed of three registered multiplier-adders concatenated into a one-dimensional systolic array. Utilizing two's complement representation, the TMC2243 accepts one 10-bit data point, updates one 10-bit coefficient, and produces one 16-bit rounded, filtered output point every 50 nanoseconds.

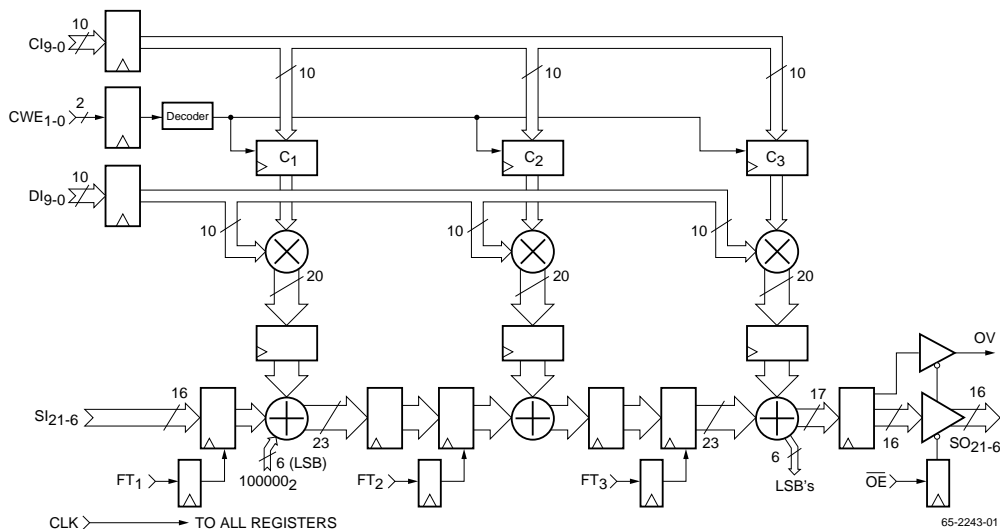
The TMC2243 has features which facilitate longer FIR filters: a 16-bit SUM-In port and user programmable pipeline registers. Enabling these registers allows the insertion of a zero-coefficient stage before each regular filter stage for up to six stages per TMC2243. Larger FIR filters can be built by

cascading Sum-In and Sum-Out.

Coefficients are stored in 3 registers and are addressed via the 2-bit Write Enable control, allowing one coefficient to be changed per clock cycle. All Data, Sum-In, Sum-Out and instruction inputs are registered on the rising edge of clock.

The 16 bits below the MSB of the 23-bit internal summation path are available at the SUM-In and Sum-Out ports. Six bits of cumulative word growth are provided internally. Data Overflow is indicated by an output flag.

Block Diagram



Functional Description

General Information

The TMC2243 consists of three identical arithmetic cells, each of which contains a 10 x 10 two's complement multiplier and a 23-bit adder. Each cell receives the current data (DI) from the Data input register, multiplies it by a locally stored Coefficient (CI_i), and adds it to the Sum SI_(i-1) received from the previous cell. The result,

$$SI_i = DI \times CI_i + SI_{(i-1)},$$

then goes to the next cell via two serial pipeline registers. When only one pipeline register is enabled, stages (i-1) and i are sequential. When both registers are enabled, there is a stage with a zero coefficient between them.

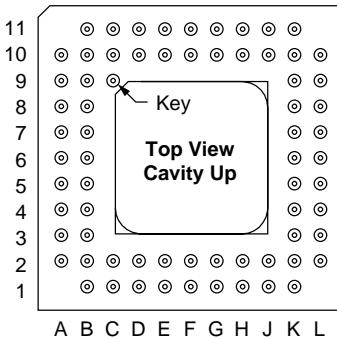
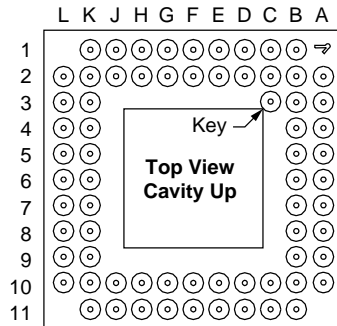
The input arithmetic cell receives SI_(i-1) via the 16-bit Sum-In port (registered when FT₁ = LOW), filling the six lower bits with 100 000 (1/2 LSB) for internal rounding. The output cell outputs 16 of the MSBs (V₂₁ through V₆) of SO_i through a register to the Sum-Out port. The Overflow flag is set when the final output exceeds 16 bits and resets with the output of the next nonoverflowing result. Sum-Out and the Overflow Flag can be forced to high-impedance with the Output Enable control. See Figure 1.

The two-bit Write Enable control specifies the loading of the three coefficient registers (one per arithmetic cell) with data appearing at the Coefficient Input port.

Pin Assignments

68 Pin Grid Array – G8 Package

69 Pin Plastic Pin Grid Array – H8 Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
A2	SO6	B9	SO20	F10	SI11	K4	CI2
A3	SO7	B10	OV	F11	SI10	K5	CI4
A4	SO9	B11	GND	G1	DI6	K6	VDD
A5	SO11	C1	FT0	G2	DI7	K7	CI7
A6	SO13	C2	OE	G10	SI13	K8	CI9
A7	SO15	C10	VDD	G11	SI12	K9	SI20
A8	SO17	C11	VDD	H1	DI4	K10	GND
A9	SO19	D1	FT2	H2	DI5	K11	SI18
A10	SO21	D2	FT1	H10	SI15	L2	DI0
B1	VDD	D10	SI7	H11	SI14	L3	CI1
B2	GND	D11	SI6	J1	DI2	L4	CI3
B3	SO8	E1	CWE1	J2	DI3	L5	CI5
B4	SO10	E2	CWE0	J10	SI17	L6	CI6
B5	SO12	E10	SI9	J11	SI16	L7	CI8
B6	SO14	E11	SI8	K1	GND	L8	SI21
B7	SO16	F1	DI8	K2	DI1	L9	SI19
B8	SO18	F2	DI9	K3	CI0	L10	CLK

Note: Pin C3 is a mechanical orientation pin on the H8 package at manufacturer's option.

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Pin Name	Pin Number	Description
Power		
VDD	B1, K6, C10, C11	Supply Voltage. The TMC2243 operates from a single +5V supply.
GND	B2, K1, K10, B11	Ground.
Inputs		
DI9-0	F2, F1, G2, G1, H2, H1, J2, J1, K2, L2	Data Input. DI9 through DI0 is the 10-bit registered Data Input; DI9 is the MSB (sign bit) and DI0 is the LSB. Data is in two's complement representation, and is clocked into the data register on each rising edge of clock. See Figure 1.
SI21-6	L8, K9, L9, K11, J10, J11, H10, H11, G10, G11, F10, F11, E10, E11, D10, D11	Sum Input. SI21 through SI6 is the 16-bit Sum-In port. SI21 is the MSB (sign bit). Sum-In is truncated to bit SI6 (plus the 1/2 LSB rounding bit in SI5) and is in two's complement representation. See Figure 1. The Sum-In port is registered, on the rising edge of clock, only when FT1 =LOW. Unique input setup requirements must be observed when operating in the feedthrough mode (FT1 = HIGH) See text.
CI9-0	K8, L7, K7, L6, L5, K5, L4, K4, L3, K3	Coefficient Input. CI9 through CI0 is the 10-bit registered Coefficient Input; CI9 is the MSB (sign bit) and CI0 is the LSB. Each coefficient and its write enable address (CWE1-3) are registered on the same clock. The coefficient is then latched into the indicated register (C1-3) at the rising edge of the next clock. The contents of this bus are ignored if a coefficient register is not selected (CWE = 00). The format of CI9-0 is identical to that of DI9-0.
Outputs		
SO21-6	A10, B9, A9, B8, A8, B7, A7, B6, A6, B5, A5, B4, A4, B3, A3, A2	Sum Output. SO21 through SO6 is the three-state 16-bit registered Sum-Out port; SO21 is the MSB (sign bit). For maximum precision, the internal products and accumulations are 23 bits but Sum-Out is internally truncated to 16 bits, and excludes the overflow bit and the 6 LSBs. The format is identical to that of SI21-6. See Figure 1.
Clock		
CLK	L10	Master Clock. The TMC2243 has a single clock input. The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of clock.
Controls		
CWE1-0	E1, E2	Coefficient Write Enable. The two bits of the registered Coefficient Write Enable control indicate which of the coefficient registers is to receive a new coefficient at the beginning of the next clock cycle. CWE1-0 Coefficient Register Selected 0 0 Holds all coefficients unchanged. 0 1 C ₁ 1 0 C ₂ 1 1 C ₃
FT3-1	D1, D2, C1	Feedthrough. These registered Feed Through controls select clocked (FT _i = LOW) or feedthrough (FT _i = HIGH) operation for each of the pipeline registers. Setting FT _i = LOW inserts a zero coefficient stage, or additional register, before the ith non-zero stage.
\overline{OE}	C2	Output Enable. Output Enable is a registered three-state enable control which forces the Sum-Out port and Overflow to the high-impedance state when HIGH. These outputs are enabled when \overline{OE} is LOW.
Flags		
OV	B10	Overflow. The Overflow Flag is a registered three-state output which goes HIGH whenever the summation result exceeds 16 bits and is reset to LOW on the next nonoverflowing result.

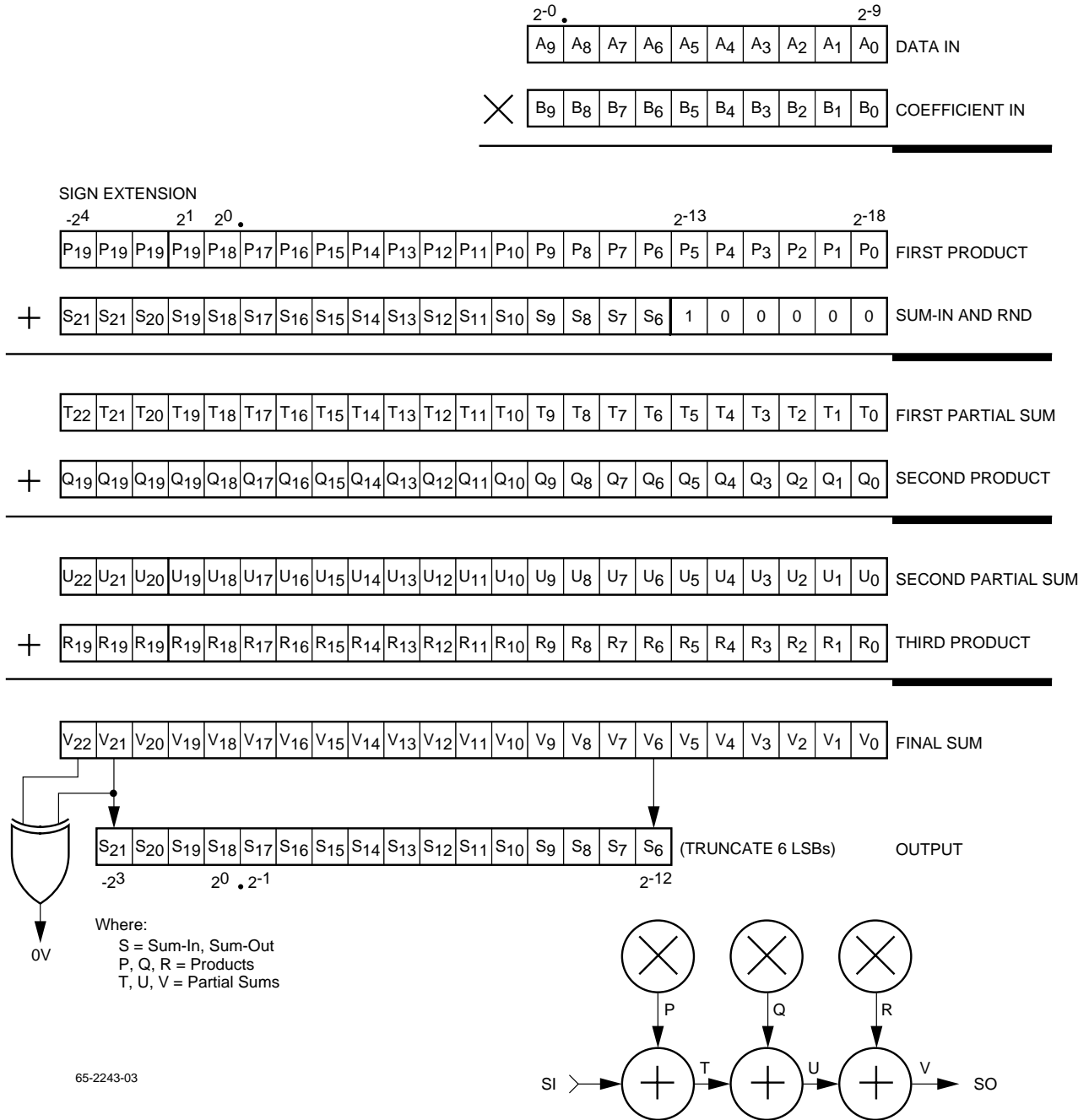
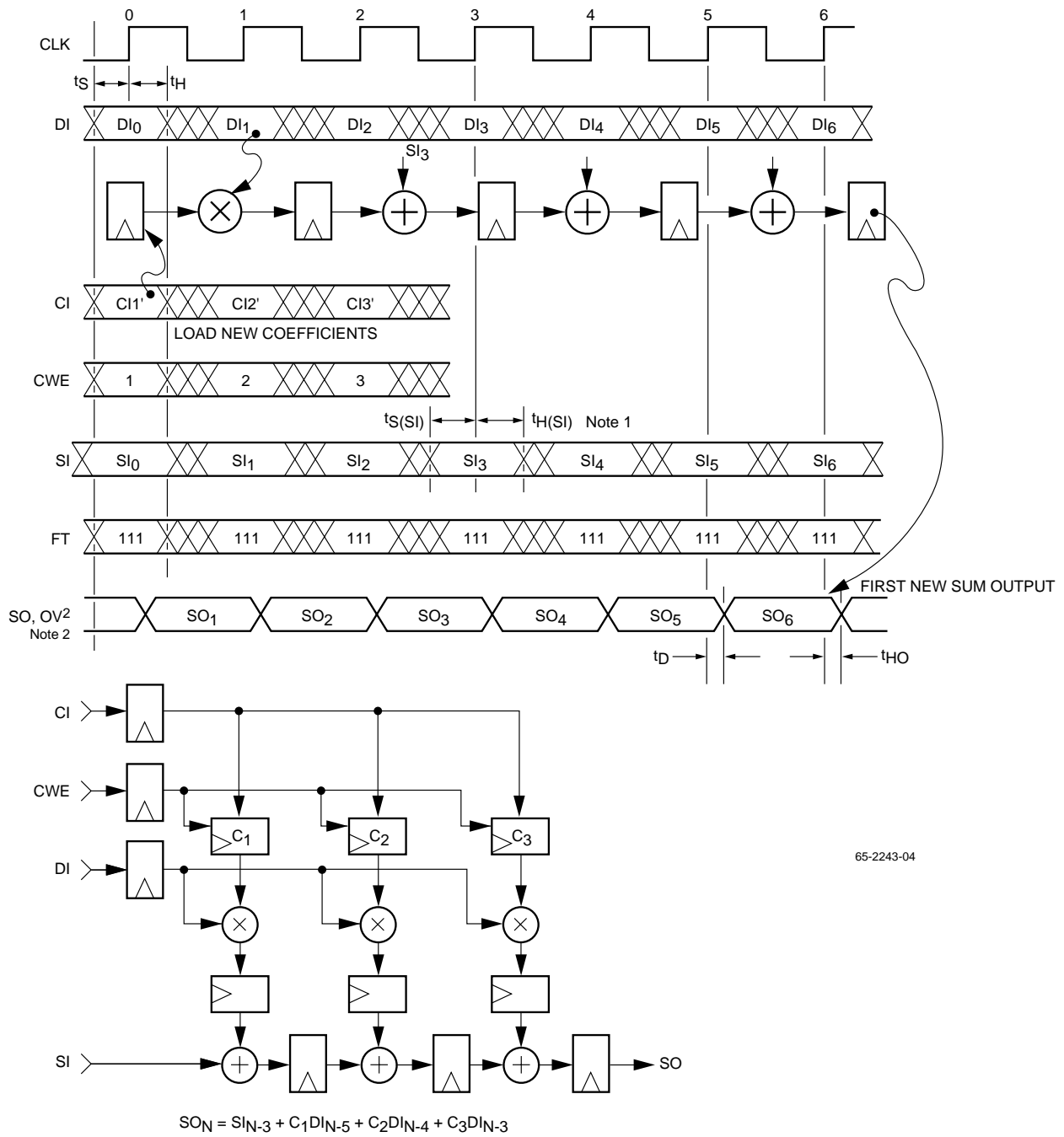


Figure 1. Data Formats and Internal Busing

Because the Sum-In and Sum-Out are truncated by 6 bits relative to the external accumulation pipeline, the TMC2243 rounds internally by adding 2^{-13} to each emerging sum of

products, effecting half-LSB rounding relative to the output format. The chip internally utilizes all lower-order bits, to 2^{-18} .

Basic Operation



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Notes:

1. Setup and Hold requirements for the Sum Input are similar to the other registered inputs when $FT_1 = LOW$. See text.
2. Sum Out and Overflow timing are shown with $\overline{OE} = LOW$.

Figure 2. Timing Diagram Demonstrating Basic Operation with $FT_{1-3} = HIGH$ (no zero stages)

The basic equation describing the function of the TMC2243 operating in a fixed state is:

$$\begin{aligned} SO(N) = & SI(N - 6 + FT1 + FT2 + FT3) \\ & + C_1 \times DI(N - 7 + FT2 + FT3) \\ & + C_2 \times DI(N - 5 + FT3) \\ & + C_3 \times DI(N - 3) \end{aligned}$$

Careful observation of the clock delays shown is basic to construction of a filter algorithm. The operating sequence for the common application with $FT_{1-3} = \text{HIGH}$ (no zero stages) is shown in Figure 2. The simplified block diagram demonstrates the clock stages in this configuration. When $FT_1 = \text{HIGH}$, the input feedthrough register is bypassed, and care must be taken to observe the setup requirements on the input of the first adder. Due to the absence of the input register buffer, note that the adder operates on data stable just prior to the arrival of the next clock, and not that setup at the rising edge of the current clock. When $FT_1 = \text{LOW}$ the input register latches the input data, and the Sum Input follows

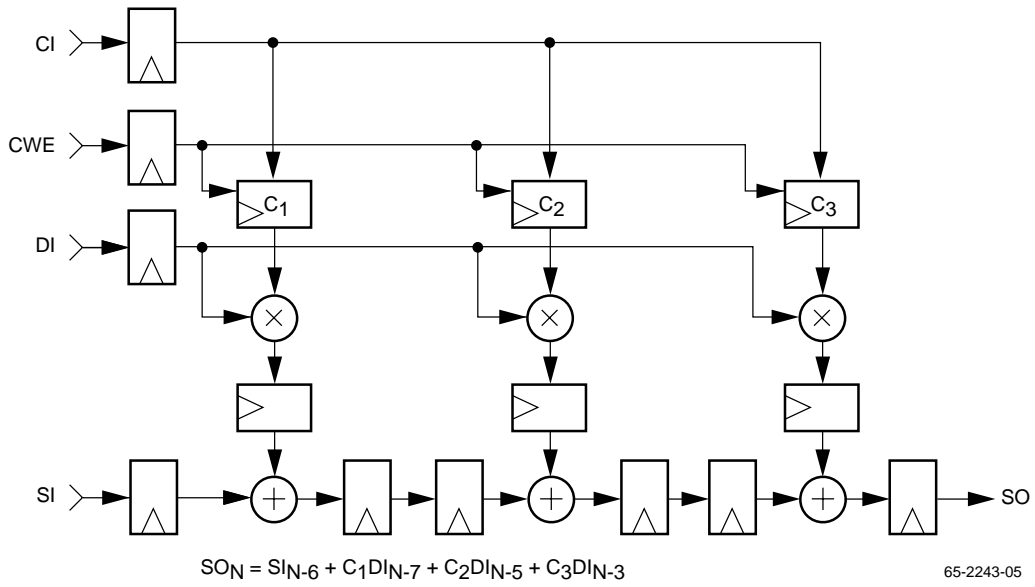
setup and hold requirements similar to the other registered inputs of the TMC2243. When $FT_1 = \text{HIGH}$, $t_S(SI)$ is guaranteed to allow 20MHz pipelined operation, assuming that input setup is observed, including cascaded operation. See the AC Characteristics table and Figure 9 in the Applications Discussion section.

Figure 3 shows the effects of the feedthrough registers on filter operation, with two different configurations. The inputs are those presented at the corresponding rising edge of clock, excepting the delayed setup requirements of the Sum Input when $FT_1 = \text{HIGH}$. The outputs are those available up to and including the corresponding edge of clock. Applications utilizing the TMC2243's ability to modify coefficients dynamically are demonstrated in Figure 4, showing the operation of a typical adaptive filter. Note that the Sum Output will be zero in the first few clock cycles of all examples only if the Coefficient Registers are initialized to zero beforehand.

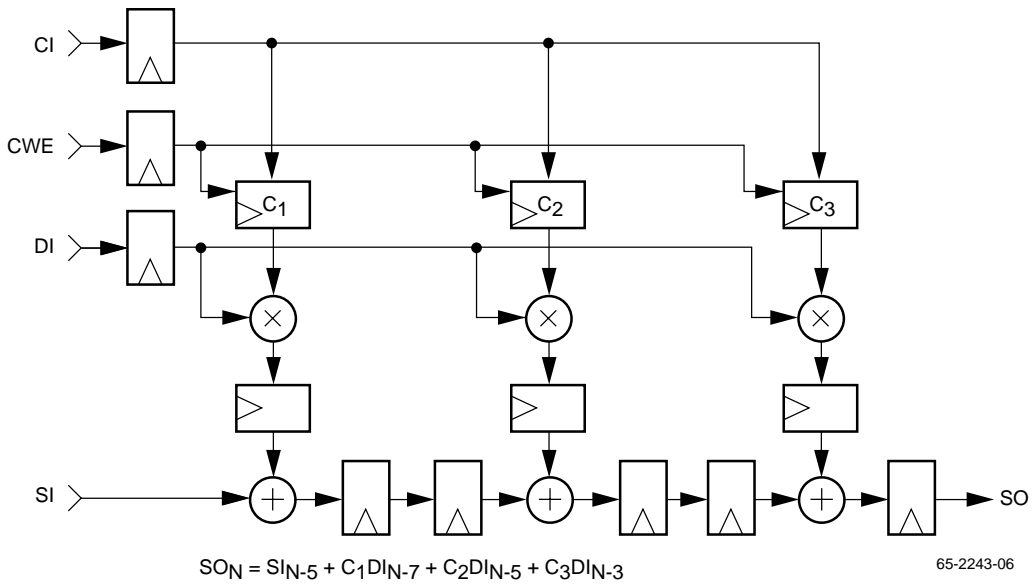
Cycle	SI(A) $FT_1 = \text{LOW}$	SI(B) $FT_1 = \text{HIGH}$	DI	CI	CWE	SO
1	0	0	0	K0	01	X
2	0	0	0	K1	10	X
3	0	0	0	K2	11	X
4	SI ₀	0	DI ₀	0	00	X
5	SI ₁	SI ₀	DI ₁	0	00	0
6	SI ₂	SI ₁	DI ₂	0	00	0
7	SI ₃	SI ₂	DI ₃	0	00	DI ₀ K ₂
8	SI ₄	SI ₃	DI ₄	K ₀ '	01	DI ₁ K ₂
9	SI ₅	SI ₄	DI ₅	0	00	DI ₀ K ₁ + DI ₂ K ₂
10	SI ₆	SI ₅	DI ₆	K ₁ '	10	SI ₀ + DI ₁ K ₁ + DI ₃ K ₂
11	SI ₇	SI ₆	DI ₇	0	00	SI ₁ + DI ₀ K ₀ + DI ₂ K ₁ + DI ₄ K ₂
12	SI ₈	SI ₇	DI ₈	K ₂ '	11	SI ₂ + DI ₁ K ₀ + DI ₃ K ₁ + DI ₅ K ₂
13	SI ₉	SI ₈	DI ₉	0	00	SI ₃ + DI ₂ K ₀ + DI ₄ K ₁ + DI ₆ K ₂
14	0	SI ₉	0	0	00	SI ₄ + DI ₃ K ₀ + DI ₅ K ₁ + DI ₇ K ₂
15	0	0	0	0	00	SI ₅ + DI ₄ K ₀ + DI ₆ K ₁ + DI ₈ K ₂
16	0	0	0	0	00	SI ₆ + DI ₅ K ₀ ' + DI ₇ K ₁ ' + DI ₉ K ₂ '
17	0	0	0	0	00	SI ₇ + DI ₆ K ₀ ' + DI ₈ K ₁ '
18	0	0	0	0	00	SI ₈ + DI ₇ K ₀ ' + DI ₉ K ₁ '
19	0	0	0	0	00	SI ₉ + DI ₈ K ₀ '
20	0	0	0	0	00	DI ₉ K ₀ '
21	0	0	0	0	00	0

Figure 3. Impulse Response Filter Operation Sequence with $FT_{2,3} = \text{LOW}$

SI(A) is the sequence of Sum Input data with $FT_{1-3} = \text{LOW}$ (three zero stages).



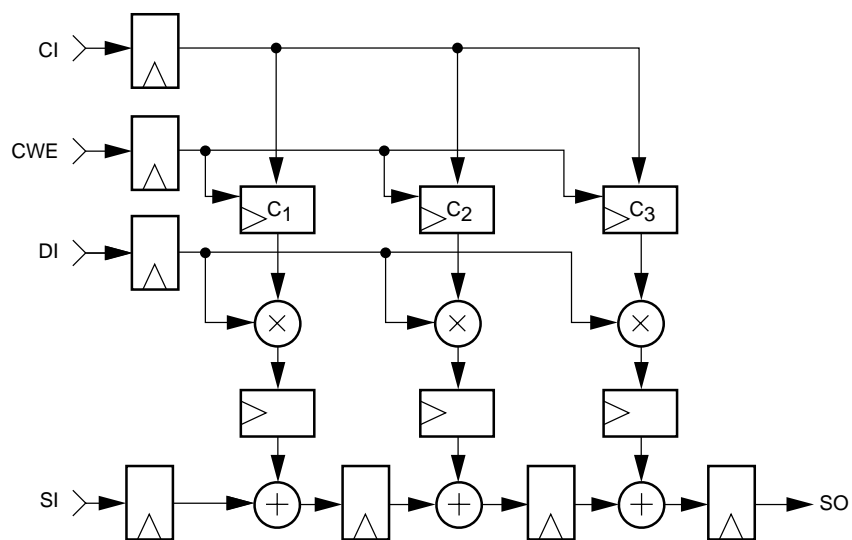
SI(B) is the sequence of Sum Input data with $FT_1 = \text{HIGH}$ and $FT_{2,3} = \text{LOW}$ (two zero stages).



Cycle	SI	DI	CI	CWE	SO
0	SI ₀	DI ₀	A ₁	01	X
1	SI ₁	DI ₁	A ₂	10	X
2	SI ₂	DI ₂	A ₃	11	X
3	SI ₃	DI ₃	B ₁	01	X
4	SI ₄	DI ₄	B ₂	10	X
5	SI ₅	DI ₅	B ₃	11	X
6	SI ₆	DI ₆	C ₁	01	SI ₂ + A ₁ DI ₁ + A ₂ DI ₂ + A ₃ DI ₃
7	SI ₇	DI ₇	C ₂	10	SI ₃ + A ₁ DI ₂ + A ₂ DI ₃ + A ₃ DI ₄
8	SI ₈	DI ₈	C ₃	11	SI ₄ + A ₁ DI ₃ + A ₂ DI ₄ + A ₃ DI ₅
9	SI ₉	DI ₉		00	SI ₅ + B ₁ DI ₄ + B ₂ DI ₅ + B ₃ DI ₆
10	SI ₁₀	DI ₁₀		00	SI ₆ + B ₁ DI ₅ + B ₂ DI ₆ + B ₃ DI ₇
11	SI ₁₁	DI ₁₁		00	SI ₇ + B ₁ DI ₆ + B ₂ DI ₇ + B ₃ DI ₈
12	SI ₁₂	DI ₁₂		00	SI ₈ + C ₁ DI ₇ + C ₂ DI ₈ + C ₃ DI ₉
13	SI ₁₃	DI ₁₃		00	SI ₉ + C ₁ DI ₈ + C ₂ DI ₉ + C ₃ DI ₁₀

Figure 4. Typical Adaptive Filter Operation Sequence

with FT₁ = LOW and FT_{2,3} = HIGH (one zero stage)



$$SO_N = SI_{N-4} + C_1DI_{N-5} + C_2DI_{N-4} + C_3DI_{N-3}$$

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Equivalent Circuits and Transition Levels

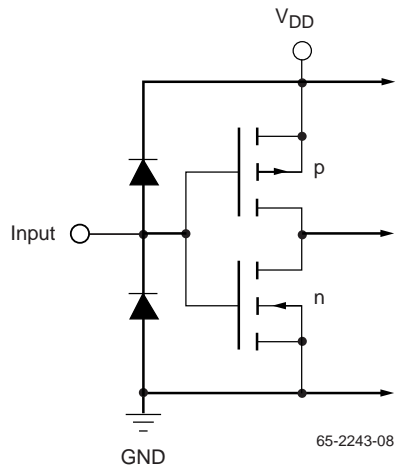


Figure 5. Equivalent Input Circuit

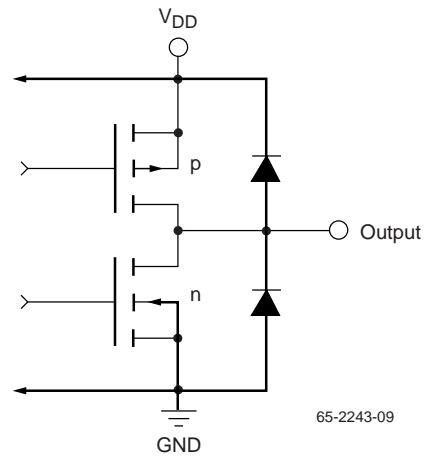


Figure 6. Equivalent Output Circuit

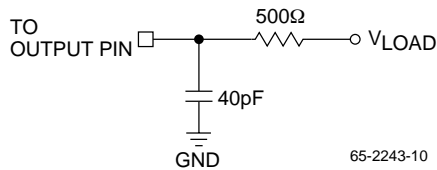
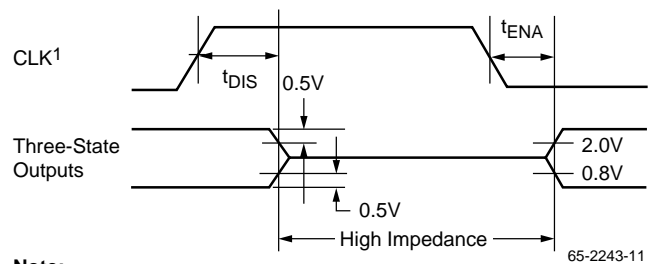


Figure 7. Test Load



Note:

1. Assumes \overline{OE} has gone LOW, within the Input Setup requirements.

Figure 8. Transition Levels for Three-State Measurements

Absolute Maximum Ratings (beyond which the device may be damaged)¹

Parameter	Min	Max	Unit
Supply Voltage	-0.5	7.0	V
Input Voltage	-0.5	VDD + 0.5	V
Output Applied Voltage ²	0.5	VDD + 0.5	V
Output Forced Current ^{3,4}	-1.0	6.0	mA
Short circuit duration (single output in HIGH state to ground)		1	sec
Operating, Case Temperature	-60	130	°C
Operating, Junction Temperature		175	°C
Storage Temperature	-65	150	°C
Lead Soldering Temperature (10 seconds)		300	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Test Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Nom	Max	Min	Nom	Max	
V _{DD}	Supply Voltage		4.75	5.0	5.25	4.5	5.0	5.5	V
V _{IL}	Input Voltage, Logic LOW		2.0			2.0			V
V _{IH}	Input Voltage, Logic HIGH				0.8			0.8	V
I _{OL}	Output Current, Logic LOW				4.0			4.0	mA
I _{OH}	Output Current, Logic HIGH				-2.0			-2.0	mA
t _{CY}	Cycle Time	V _{DD} = Min	50			50			ns
t _{PWL}	Clock Pulse Width LOW	V _{DD} = Min	20			20			ns
t _{PWH}	Clock Pulse Width HIGH	V _{DD} = Min	20			20			ns
t _S	Input Setup Time		15			20			ns
t _{S(SI)}	Input Setup Time	Sl ₂₁₋₆ , FT ₁ = HIGH	25			28			ns
		FT ₁ = LOW	18			20			ns
t _H	Input Hold Time		2			3			ns
t _{H(SI)}	Input Hold Time, Sl ₂₁₋₆		5			5			ns
T _A	Ambient Temperature, Still Air		0		70				°C
T _C	Case Temperature					-55		125	°C

DC Characteristics¹

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I _{DDQ}	Supply Current, Quiescent	V _{DD} = Max, V _{IN} = OV, \overline{OE} = HIGH		15		15	mA
I _{DDU}	Supply Current, Unloaded	V _{DD} = Max, \overline{OE} = HIGH f = 20MHz		90		90	mA
				48		48	mA
I _{IL}	Input Current, Logic LOW	V _{DD} = Max, V _{IN} = OV	-75	75	-75	75	μA
I _{IH}	Input Current, Logic HIGH	V _{DD} = Max, V _{IN} = V _{DD}	-75	75	-75	75	μA
V _{OL}	Output Voltage, Logic LOW	V _{DD} = Min, I _{OL} = Max		0.4		0.4	V
V _{OH}	Output Voltage, Logic HIGH	V _{DD} = Min, I _{OH} = Max	2.4		2.4		V
I _{OZL}	Hi-Z Output Leakage Current, Output LOW	V _{DD} = Max, V _{IN} = OV	-40	40	-40	40	μA
I _{OZH}	Hi-Z Output Leakage Current, Output HIGH	V _{DD} = Max, V _{IN} = V _{DD}	-40	40	-40	40	μA
I _{OS}	Short-Circuit Output Current	V _{DD} = Max, Output HIGH, one pin to ground, one second duration max		-150		-150	mA
C _I	Input Capacitance	T _A = 25°C, f = 1MHz		10		10	pF
C _O	Input Capacitance	T _A = 25°C, f = 1MHz		10		10	pF

Note:

1. Actual test conditions may vary from those shown, but guarantee operation as specified.

AC Characteristics

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t _D	Output Delay	V _{DD} = Min, C _{LOAD} = 40pF		30		30	ns
t _{DC}	Output Delay, Cascaded	V _{DD} = Min, C _{LOAD} = 10pF		20		20	ns
t _{HO}	Output Hold Time	V _{DD} = Max, C _{LOAD} = 40pF	5		5		ns
t _{ENA}	Three-State Output, Enable Delay ¹	V _{DD} = Min, C _{LOAD} = 40pF		20		25	ns
t _{DIS}	Three-State Output, Disable Delay ¹	V _{DD} = Min, C _{LOAD} = 40pF		15		20	ns

Note:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Application Discussion

Loading and Updating of Coefficients

Because of the TMC2243’s internal architecture, its impulse response is C₃, C₂, C₁, where C₃ is the rightmost coefficient and C₁ is the leftmost. However, for glitchless performance, coefficients must be updated from left to right: C₁ then C₂ then C₃.

For example, consider an adaptive filter whose first set of coefficients is A_i, second set is B_i and third set is C_i (Figure 4). First, the TMC2243 is initialized with A_i. If these are loaded in numerical (left to right) sequence, two of the first three data points can be loaded with them, as shown in Figure 4. Immediately after the third coefficient is loaded, the first coefficient of the next set can be loaded, if desired, along with the third data point.

Table 1. Impulse Response

FT ₃₋₁	Response					
000	C ₃	0	C ₂	0	C ₁	0
001	C ₃	0	C ₂	0	C ₁	
010	C ₃	0	C ₂	C ₁	0	
011	C ₃	0	C ₂	C ₁		
100	C ₃	C ₂	0	C ₁	0	
101	C ₃	C ₂	0	C ₁		
110	C ₃	C ₂	C ₁	0		
111	C ₃	C ₂	C ₁			

Notes:

1. C₃ is the rightmost coefficient, C₁ is the leftmost
2. FT₁ is relevant only if SUMIN is used. When multiple chips are cascaded, FT₁ LOW places a zero stage between their concatenated impulse responses.

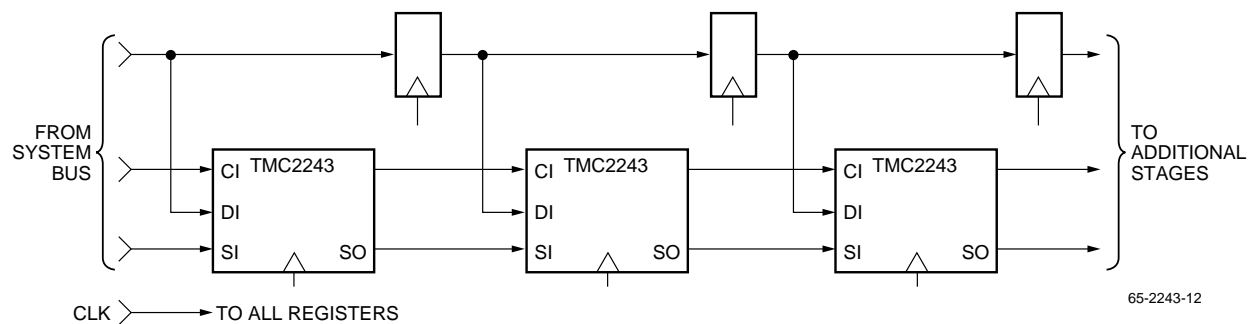
Building Longer Filters

To build a filter of more than three non-zero stages, merely concatenate a series of TMC2243s. The coefficient inputs may be connected to the data bus, a separate common coefficient bus, or separate buses, depending on system architecture, memory and bus resources, and coefficient updating requirements. The data inputs are connected to a common bus. If the first feedthrough register is used (and a zero stage is not desired there), an external register should be inserted in the data input path for proper timing (Figure 9).

The 16-bit Sum-Out port of each TMC2243 is connected to the Sum-In port of the next TMC2243 in the chain; the filter output is the Sum-Out port of the last TMC2243. Since the 6 LSBs of each TMC2243’s accumulation pipeline are not output, each TMC2243 incorporates a rounding increment of 1 into the sixth bit, to minimize bias.

When TMC2243s are cascaded in this fashion, the minimum permissible clock period is the sum of the output delay and the Sum-In port’s input setup time. When the Input Registers are enabled (that is, FT₁ = LOW), full 20MHz performance can be obtained.

All data and coefficient inputs and outputs are two's complement representation, whose relative scaling is presented in the Data Formats table, Figure 1. Although the data values are shown in fractional format, the user can arbitrarily rescale them, as long as consistency is maintained.



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Figure 9. Basic Diagram for Stacking the TMC2243 for High-Speed Operation (no zero tap desired between each TMC2243, all FT₁ = LOW)

Notes:

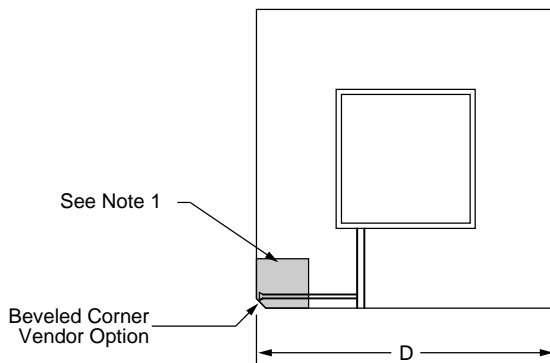
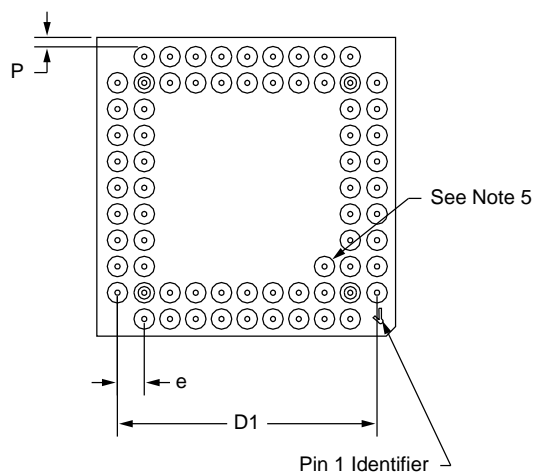
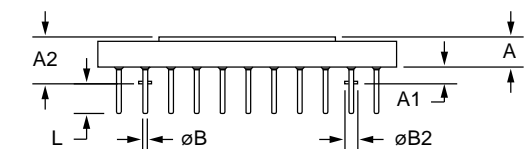
Mechanical Dimensions

68 Lead PGA Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.125	2.03	3.18	
A1	.040	.060	1.02	1.52	
A2	.115	.190	2.92	4.83	
øB	.017	.020	0.43	0.51	
øB2	.050 NOM.		1.27 NOM.		
D	1.140	1.180	28.96	29.97	
D1	1.000 BSC		25.40 BSC		
e	.100 BSC		2.54 BSC		
L	.120	.140	3.05	3.56	
M	11		11		2
N	68		68		3
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Dimension "M" defines matrix size.
3. Dimension "N" defines the maximum possible number of pins.
4. Controlling dimension: inch.
5. Optional index pin.



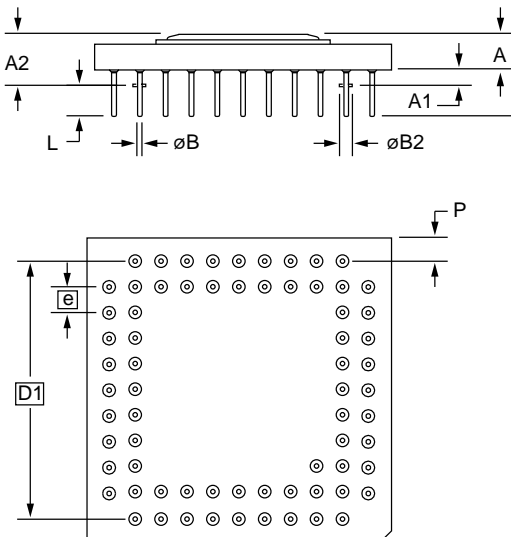
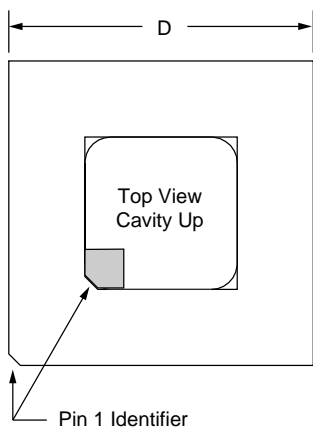
Mechanical Dimensions (continued)

69 Lead PGA Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.140	1.180	28.96	29.97	SQ
D1	1.000 BSC		25.40 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
M	11		11		3
N	68		68		4
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2243G8C	STD- $T_A = 0^{\circ}\text{C}$ to 70°C	Commercial	68 Pin Grid Array	2243G8C
TMC2243G8V	EXT- $T_C = 55^{\circ}\text{C}$ to 125°C	MIL-STD-883	68 Pin Grid Array	2243G8V
TMC2243H8C	STD- $T_A = 0^{\circ}\text{C}$ to 70°C	Commercial	69 Pin Plastic Pin Grid Array	2243H8C

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.